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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,320	SEKI, HAJIME	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention without undue experimentation. Specifically Applicant has not enabled how to build a stack in a circular manner without undue experimentation. A stack grows ands shrinks from the same end. In a stack nothing circular is needed. Appropriate correction is required.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 16 depends from cancelled claim 7. For the purposes of this Office Action it is assumed that claim 16 depends from claim 15 instead. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that

the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeager et al., US Patent 5,758,112, in view of Walker, US Patent 5,881,305.

7. Referring to claim 9, Yeager et al. have taught a computer system for executing programs described in a machine language based on stack architecture, comprising:

a. a data cache (Figure 1, element 424);

b. a data buffer that can hold data of variables (Figure 1, elements 428 and 430);

c. a consolidated register file each entry of which is designed to hold data (Figure 1, elements 302 and 306);

d. an advanced pointer stack each entry of which is designed to hold an entry address in said consolidated register file (Figure 1, elements 204 and 206, column 6, lines 35-53);

e. an instruction buffer of a FIFO queue each entry of which is designed to hold the substance of an instruction (Figure 2, active list, element 212, column 5, line 45-column 6, line 13);

f. an arithmetic/logic unit that is designed to execute arithmetic/logic operations (Figure 1, elements 412 and 414); and

g. a load/store unit that can access said data cache and said data buffer (Figure 1, element 416, column 5, lines 23-30) wherein;

8. Yeager et al. have not specifically taught the advanced pointer memory area being an advanced pointer stack. Walker has taught an advanced pointer stack (Walker, abstract, column 16, lines 54-column 17, line 3) for the desirable purpose of employing less storage space for each

register rename map. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the advanced pointer memory area of Yeager et al., be implemented as a stack, as taught by Walker, for the desirable purpose of employing less storage space for each register rename map (Walker, abstract, column 16, lines 54-column 17, line 3).

9. Combining Yeager et al. with Walker necessarily yields wherein,

a. entry addresses in said consolidated register file, to be popped, are popped from said advanced pointer stack when an instruction including a pop operation from an operand stack is decoded (Walker, abstract, column 16, lines 54-column 17, line 3);

b. entries of said consolidated register file that have not been allocated are allocated, to the number of words to be pushed, and the addresses of said newly allocated entries of said consolidated register file are pushed onto said advanced pointer stack when an instruction including a push operation onto the operand stack is decoded (Walker, abstract, column 16, lines 54-column 17, line 3);

c. the substance of each decoded instruction, together with the popped/pushed entry addresses in said consolidated register file, when the instruction includes a pop / push operation, is written into said instruction buffer (Yeager et al., column 6, line 65-column 7, line 17); and

d. unexecuted instructions held in said instruction buffer are to be executed using the data driven principle (Yeager et al., column 6, line 65-column 7, line17).

10. Referring to claim 10, Yeager et al. have taught the computer system according to claim 9, further comprising:

a. a completed pointer stack each entry of which is designed to hold an entry address in said consolidated register file (Yeager et al., column 6, lines 7-13), wherein:

b. said completed pointer stack is manipulated so as to reproduce the operation that was applied on said advanced pointer stack in the course of decoding of said instruction when the instruction held in the head entry of said instruction buffer is/becomes ready to be completed, in accordance with the substance in said head entry of said instruction buffer, and said head entry is dequeued (Yeager et al., column 6, lines 7-13); and

c. each entry of said consolidated register file whose address said completed pointer stack loses hold of on account of a pop operation is released from allocation (Yeager et al., column 6, lines 7-13).

11. Referring to claim 11, Yeager et al. have taught the computer system according to claim 10, further comprising:

a. a free list that is designed to hold addresses of free entries of said consolidated register file (Figure 1, element 210, column 7, lines 60-63), wherein:

b. in the initialized state, the addresses of all the entries of said consolidated register file are registered on said free list (Yeager et al., column 12, lines 24-67);

c. an address of free entry of said consolidated register file is taken out of said free list, when an entry of said consolidated register file needs to be allocated (Yeager et al., column 12, lines 24-67); and

d. the address of each entry of said consolidated register file that is released from allocation is to be registered on said free list (Yeager et al., column 12, lines 24-67).

12. Referring to claim 12, Yeager et al. have taught the computer system according to claim 10, further comprising:

a. an advanced pointer stack history file each entry of which is designed to hold the contents of said advanced pointer stack (column 17, lines 62-67), wherein:

b. each entry of said consolidated register file being designed to further hold a branch tag (column 17, line 50-column 18, line 20);

c. in decoding an instruction, a branch tag is written into each entry of said consolidated register file that is being allocated (column 17, line 50-column 18, line 20);

d. the contents of said advanced pointer stack are written into an entry of said advanced pointer stack history file each time a conditional branch instruction is decoded (column 17, lines 55-63), and then, with an updated branch tag, speculative execution based on branch prediction is carried out (column 17, line 50-column 18, line 20); and

e. each entry of said consolidated register file in which a branch tag for instructions decoded after said conditional branch instruction is written, in the case that a branch prediction turns out to have missed, instructions decoded after the conditional branch instruction are invalidated, is released from allocation, the contents of said advanced pointer stack history file that were written when said conditional branch instruction was decoded are copied into said advanced pointer

f. stack, and the process is resumed from the instruction at the right place (column 19, lines 14-32, column 17, lines 4-25).

13. Referring to claim 13, Yeager et al. have taught the computer system according to claim 10, wherein:

a. said advanced pointer stack and said completed pointer stack being each constructed as a circular buffer (Yeager et al., column 6, lines 7-13, Figure 1, elements 204 and 206, column 6, lines 35-53, column 15, lines 49-60);

b. the data held in the entry of said consolidated register file indicated by said identical content can be spilt into said data buffer, when the content of the bottom entry holding an entry address in said consolidated register file is identical between said advanced pointer stack and said completed pointer stack, with the hold of the entry address in said consolidated register file in said bottom entry removed both in said advanced pointer stack and in said completed pointer stack (Figure 1, elements 204 and 206, column 6, lines 35-53, Figure 2, active list, element 212, column 5, line 45-column 6, line 13, A graduating instruction.); and

c. said consolidated register file can be filled with data from said data buffer by allocating a free entry of said consolidated register file to said data, writing said data into said entry, and having the entry under the bottom entry holding an entry address in said consolidated register file hold the address of said entry of said consolidated register file into which said data is being written both in said advanced pointer stack and in said completed pointer stack (Figure 1, elements 204 and 206, column 6, lines 35-53, Figure 2, active list, element 212, column 5, line 45-column 6, line 13).

14. Referring to claim 14, Yeager et al. have taught the computer system according to claim 11, wherein:

a. said free list being constructed as a FIFO queue (column 12, lines 57-63);

b. in accordance with a plurality of instructions decoded simultaneously, manipulation of said advanced pointer stack, allocation of entries of said consolidated register file, and writing of substances of said plurality of instructions into successive entries of said instruction buffer are to be conducted at a time (Figure 2, active list, element 212, column 5, line 45-column 6, line 13, column 2,, lines 55-60, column 8, lines 34-40); and

c. in accordance with substances held in a plurality of successive entries of said instruction buffer, manipulation of said completed pointer stack, and release of entries of said consolidated register file from allocation are to be conducted at a time (column 6, lines 7-13).

15. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeager et al., US Patent 5,758,112, in view of Walker, US Patent 5,881,305, and An Efficient Algorithm for exploiting Multiple Arithmetic Units, Tomasulo, R. M. (hereinafter referred to as Tomasulo).

16. Referring to claim 15, Yeager et al. have taught a computer system for executing programs described in a machine language based on stack architecture, comprising:

a. a consolidated register file each entry of which is designed to hold data (Figure 1, elements 302 and 306);

b. an advanced pointer memory area each entry of which is designed to hold an entry address in said consolidated register file (Figure 1, elements 204 and 206, column 6, lines 35-53);

c. an instruction buffer of a FIFO queue each entry of which is designed to hold the substance of an instruction (Figure 2, active list, element 212, column 5, line 45-column 6, line 13);

d. functional units each having an appropriate number of reservation stations (Figure 1, element 416, column 5, lines 23-30); and

17. Yeager et al. have not specifically taught the advanced pointer memory area being an advanced pointer stack. Walker has taught an advanced pointer stack (Walker, abstract, column 16, lines 54-column 17, line 3) for the desirable purpose of employing less storage space for each register rename map. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the advanced pointer memory area of Yeager et al., be implemented as a stack, as taught by Walker, for the desirable purpose of employing less storage space for each register rename map (Walker, abstract, column 16, lines 54-column 17, line 3).

18. Combining Yeager et al. with Walker necessarily yields entry addresses in said consolidated register file, to be popped, are popped from said advanced pointer stack when an instruction including a pop operation from an operand stack is decoded (Walker, abstract, column 16, lines 54-column 17, line 3);

a. entries of said consolidated register file that have not been allocated are allocated, to the number of words to be pushed, and the addresses of said newly allocated entries of said consolidated register file are pushed onto said advanced pointer stack when an instruction including a push operation onto the operand stack is decoded (Walker, abstract, column 16, lines 54-column 17, line 3).

b. the substance of each decoded instruction, together with the popped/pushed entry addresses in said consolidated register file when the instruction includes a pop / push operation, is written into said instruction buffer (Yeager et al., column 6, line 65-column 7, line17);

19. Yeager et al. have not taught a common data bus through which data and their respective entry addresses in said consolidated register file are to be distributed among said consolidated register file and said functional units. Tomasulo has taught a common data bus through which data and their respective entry addresses in said consolidated register file are to be distributed among said consolidated register file and said functional units (Tomasulo, Pages 30-32) for the desirable purpose of having the result of an operation immediately available to all units upon calculation. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Yeager et al. include the common data bus of Tomasulo, for the desirable purpose of having the result of an operation immediately available to all units upon calculation (Tomasulo, page 30).

20. Yeager et al. have not taught the substance of each instruction that is written into said instruction buffer is written into a free reservation station of a functional unit that is to execute the instruction, if necessary according to the type of the instruction. Tomasulo has taught the substance of each instruction that is written into said instruction buffer is written into a free reservation station of a functional unit that is to execute the instruction, if necessary according to the type of the instruction (Tomasulo, page 29) for the desirable purpose of associating more than one set of registers with each execution unit which ultimately reduces execution time. It would have been obvious to one of ordinary skill in that art at the time the invention was made to

have the invention of Yeager et al., include the claimed reservation station, as taught by Tomasulo, for the desirable purpose of associating more than one set of registers with each execution unit which ultimately reduces execution time (Tomasulo, page 29).

21. Yeager et al. in combination with Tomasulo and Walker have taught the contents of each entry of said consolidated register file whose address is popped from said advanced pointer stack are read out, and if data is already written, the entry address and the data are to be put on said common data bus (Tomasulo, page 30, Yeager et al., Figure 1, elements 302 and 306);

a. in each of said reservation stations holding substance of an instruction, each address of entry of said consolidated register file to hold source data is compared with entry addresses in said consolidated register file delivered through said common data bus, data is taken in if any matched, and said instruction is to be performed after required source data are fully arranged (Yeager et al., Figure 1, elements 204 and 206, column 6, lines 35-53, Figure 2, active list, element 212, column 5, line 45-column 6, line 13, Tomasulo, page 29);

b. each of said functional units is to put, on said common data bus, each result data produced by executing an instruction that pushes an entry address in said consolidated register file onto said advanced pointer stack when decoded, together with the pushed entry address in said consolidated register file (Tomasulo, Pages 30-32); and

c. in accordance with contents delivered through said common data bus, data are written in said consolidated register file (Figure 1, elements 302 and 306, column 5, line 45-column 6, line 13).

22. Referring to claim 16, Yeager et al. have taught the computer system according to claim 7, further comprising:

a. a completed pointer stack each entry of which is designed to hold an entry address in said consolidated register file (Yeager et al., column 6, lines 7-13), wherein;

b. said completed pointer stack is manipulated so as to reproduce the operation that was applied on said advanced pointer stack in the course of decoding of said instruction, said head entry is dequeued when the instruction held in the head entry of the queue of said instruction buffer is/becomes ready to be completed, in accordance with the substance in said head entry of said queue (Yeager et al., column 6, lines 7-13), and

c. each entry of said consolidated register file whose address said completed pointer stack loses hold of on account of a pop operation is released from allocation (Yeager et al., column 6, lines 7-13).

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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